Bake Stability of Long-Wavelength Infrared HgCdTe Photodiodes

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The bake stability was examined for HgCdTe wafers and photodiodes with CdTe surface passivation deposited by thermal evaporation. Electrical and electro-optical measurements were performed on various long-wavelength infrared HgCdTe photodiodes prior to and after a ten-day vacuum bakeout at 80°C, similar to conditions used for preparation of tactical dewar assemblies. It was found that the bakeout process generated additional defects at the CdTe/HgCdTe interface and degraded photodiode parameters such as zero bias impedance, dark current, and photocurrent. Annealing at 220°C under a Hg vapor pressure following the CdTe deposition suppressed the interface defect generation process during bakeout and stabilized HgCdTe photodiode performance.

Key words: HgCdTe photodiodes, long-wavelength infrared (LWIR) detectors, thermal annealing

INTRODUCTION

Surface passivation of HgCdTe p/n heterojunction photodiodes by thermal evaporation of CdTe has the advantages of simple operation, excellent run-to-run reproducibility, and low capital equipment requirement. The developed and implemented passivation process provides bulk defect limited photodiode performance with an excellent R_0A product at 77K close to the diffusion limit.[1-3] However, devices passivated by this technique have a tendency to degrade after an 80°C, 240 h vacuum bakeout. Analysis shows that defects, possibly electrically active Hg vacancies, generated by the bakeout process at the CdTe/HgCdTe interface are responsible for this degradation. This effect has been eliminated by the use of a post-passivation anneal at 220°C under Hg vapor pressure which, it is believed, inhibits the generation of Hg vacancies.

DEVICE FABRICATION AND TESTING

LPE Grown Photovoltaic HgCdTe Devices

Heterojunction photodiode test structures were fabricated on a liquid phase epitaxy (LPE) grown wafer following the standard process, included CdTe passivation deposition with substrate at room temperature. A second portion of this wafer was processed with an additional Hg anneal after passivation step with substrate at 155°C. This wafer consisted of an LPE grown In-doped n-type HgCdTe layer (1×10^{15} cm^{-3} donor concentration) capped by a 1 μm thick p-type layer of wider bandgap (x = 0.300) and with an acceptor concentration of 5×10^{17} cm^{-3}. The cutoff wavelength of the diodes was λ_c = 10.1 μm. One type of test die consisted of variable area square photodiodes with mesa side lengths varying from 22 to 250 μm. Another die contained a mini-array of identical diodes (22 μm mesa-side). A metal insulator semiconductor (MIS) capacitor, formed by a 500 × 200 μm field plate over the n-layer with the CdTe passivation as the insulator, was also used in the characterization.

For the photodiodes, DC dark current measurements were performed with an HP 4141B DC source/monitor. AC photo-response measurements were performed using an Electro-Optical Industries, Inc., blackbody radiation source (Model WS143) operated at a temperature of 500K and chopped at a frequency of 41.5 Hz. The signal was amplified by an EG&G 114 Signal Conditioning Amplifier and stored with a Tektronix 7854 digitizing oscilloscope. Spectral response was performed with an Optronics Laborato-

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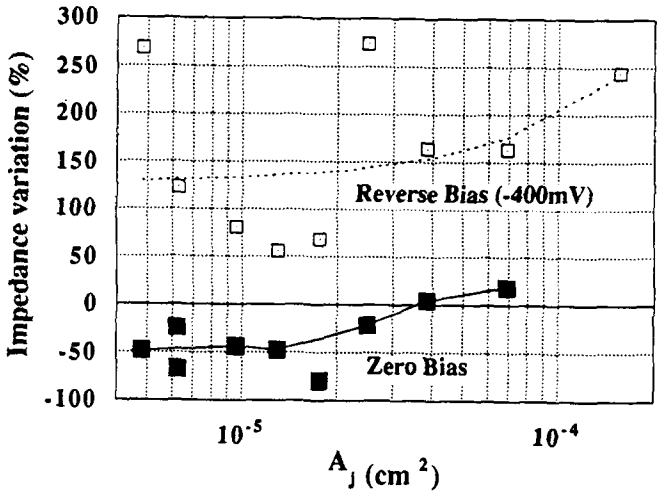


Fig. 1. Standard process sequence. Impedance variation after bakeout 240 h at 80°C.

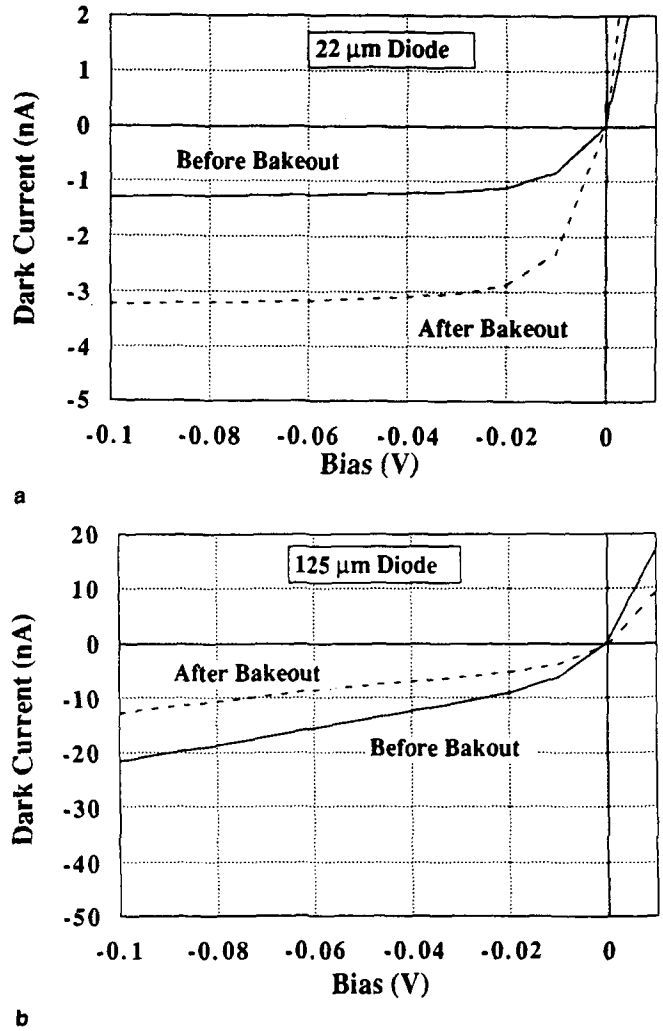


Fig. 2. (a) Standard process sequence. Dark current I-V curves before and after 240 h bakeout for 22 μm (mesa-size) diode, and (b) dark current I-V curves before and after 240 h bakeout for 125 μm (mesa-size) diode.

ries Inc., infrared spectroradiometer (Model 746-D). Capacitance-voltage (C-V) measurements of the MIS devices were made with an HP 4275 multi-frequency LCR meter.

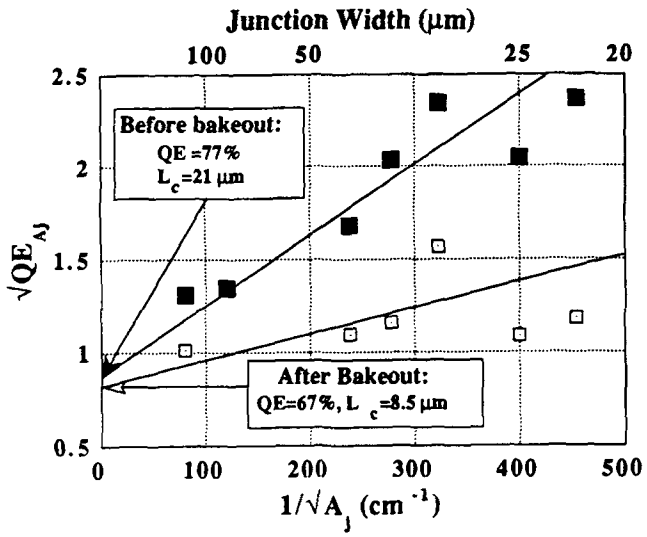


Fig. 3. Standard process squence. Quantum efficiency and collection distance before and after 240 h bakeout.

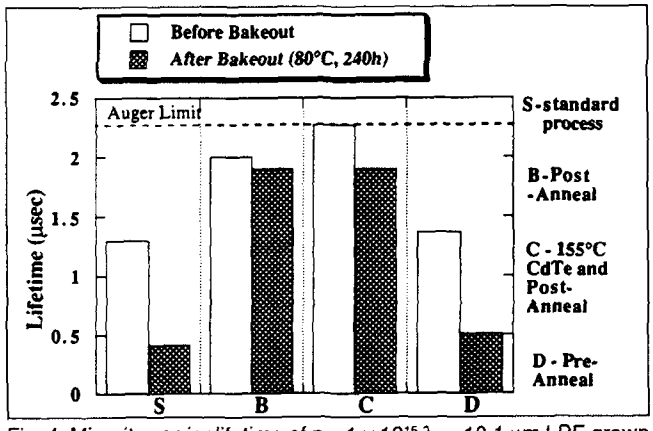


Fig. 4. Minority carrier lifetime of $n = 1 \times 10^{15}$ $\lambda_c = 10.1$ μm LPE grown HgCdTe layers passivated with thermally evaporated CdTe before and after bakeout at 80°C for 240 h.

LPE Grown HgCdTe N-Layer

An LPE-grown n-type HgCdTe layer on CdTe substrate was cleaved into four pieces. The n-layer was 20 μm thick, had a carrier concentration of 1×10^{15} cm^{-3}, a calculated Auger lifetime (τ_{Auger}) of 2.2 μs, and x = 0.215 ($Hg_{1-x}Cd_xTe$). The piece, part "S" (standard), was passivated with 5000Å of CdTe deposited at room temperature,[2] and then prepared for bakeout and measurement. Part "B" underwent the same passivation as "S" and was then annealed at 220°C under Hg vapor after the CdTe deposition.[2] Part "C" was annealed after the CdTe deposition at a substrate temperature of 155°C ("Hot" CdTe). Part "D" was annealed before passivation.

The minority carrier lifetime was measured by the photoconductive decay technique at a wavelength of 850 nm using Model 6020 Light Pulse Generator (Berkeley Nucleonics Corporation) as a radiation source. The lifetime values reported represent the average of several measurements at different locations on each sample.

Bakeout was performed in a vacuum oven at 80°C and 0.01 Torr for a total time of 240 h. A full set of characterization measurements was performed before and after completion of the bakeout. All measurements were performed at device temperatures from 77 to 80K.

EXPERIMENTAL RESULTS AND DISCUSSION

Devices Fabricated Without Anneal

The zero-bias impedance under dark (0° field of view [FOV]) conditions—one of the most important photodiode parameters—decreased after bakeout for small area diodes but increased slightly for large diodes (Fig. 1). Under strong reverse bias (–400 mV), the impedance increased after bakeout for all sizes of diodes, the largest increase being for large diodes. The impedance variation is defined as the percentage change in impedance from its initial value before bakeout to its final value after bakeout.

Figure 2 shows typical results for 0° FOV current-voltage (I-V) measurements of 22 and 125 μm diodes before and after bakeout. The dark current is observed to increase for small diodes (Fig. 2a) mostly because the saturation current increased. Both I-V curves have almost the same slope before and after bakeout for biases greater than 3 to 5 kT/q (35–40 mV). This indicates that recombination current due to bulk defects did not increase after bakeout. Meanwhile, the 125 μm diode shows defect-limited behavior, and the dark current after bakeout did not change significantly (Fig. 2b). There is no sign of increased saturation current in this case.

Analysis of the chopped blackbody photodiode response measurements for variable area diodes yields values for quantum efficiency and the lateral collection distance.[3] These results are shown in Fig. 3 where QE_{Aj} is the apparent quantum efficiency, assuming the optical and junction area are equal, and is determined by equation:

$$\sqrt{QE_{Aj}} = \sqrt{QE} + \sqrt{QE}\,\frac{2L_c}{\sqrt{A_j}}$$

where A_j is the junction area, L_c is the lateral collection distance, which is the distance beyond the junction edge from which photo-generated carriers

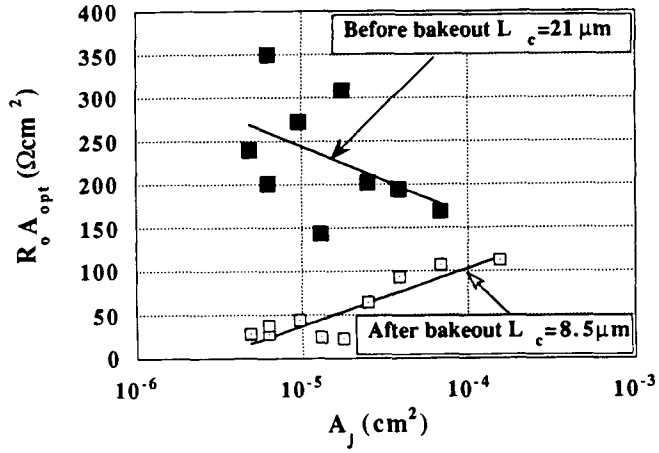


Fig. 5. Standard process sequence. R_0A_{opt} performance as a function of detector junction area before and after bakeout for 240 h at 80°C.

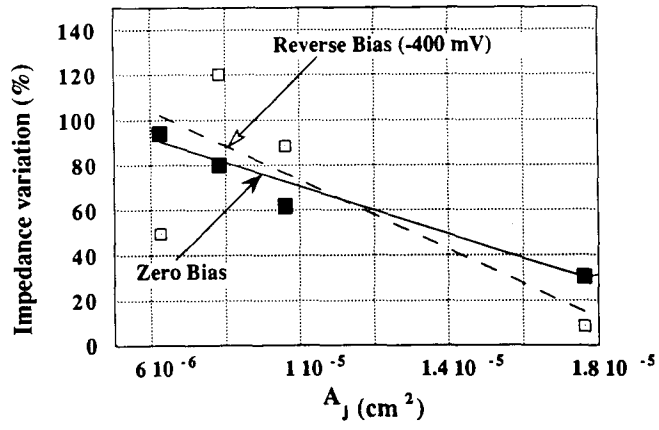
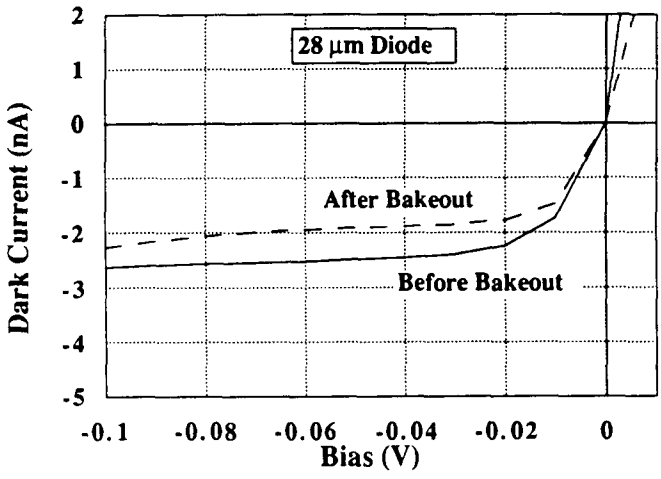


Fig. 6. CdTe deposited at 155°C followed by a Hg anneal. Impedance variation after bakeout for 240 h at 80°C.



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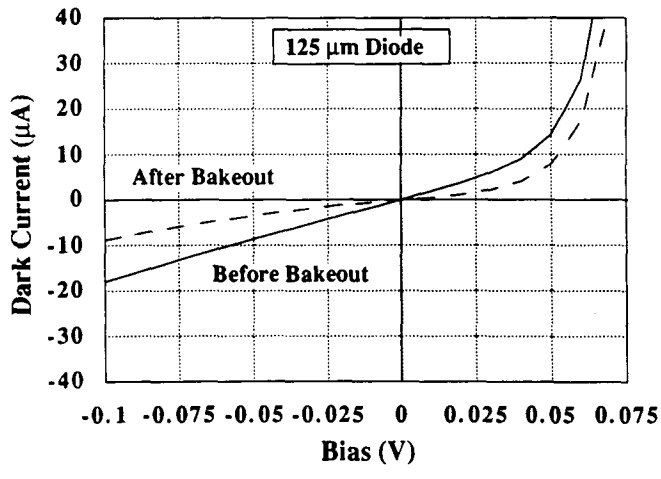

b

Fig. 7. (a) CdTe deposited at 155°C followed by a Hg anneal. Dark current I-V curves before and after 240 h bakeout for 28 μm (mesa-size) diode, and (b) CdTe deposited at 155°C followed by a Hg anneal. Dark current I-V curves before and after 240 h bakeout for 125 μm (mesa-size) diode.

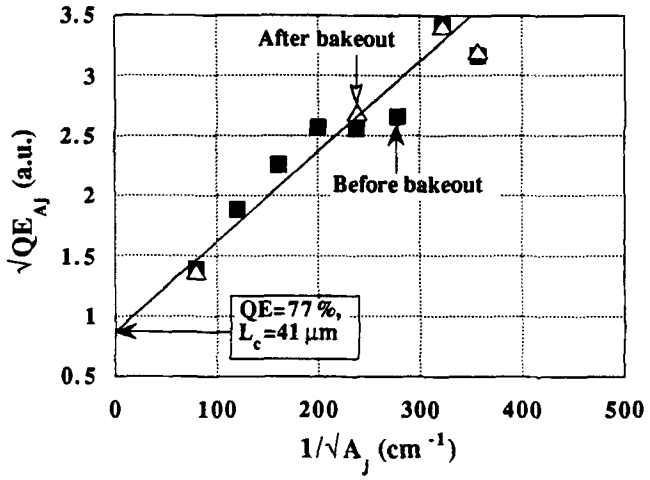

Fig. 8. CdTe depositd at 155°C followed by a Hg anneal. Quantum efficiency and collection distance before and after 240 h bakeout.

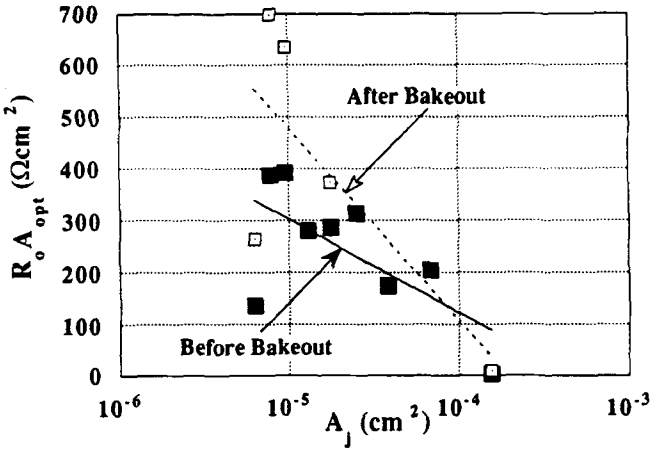

Fig. 9. CdTe deposited at 155°C followed by a Hg anneal. R_0A_{opt} performance as a function of detector junction area before and after bakeout for 240 h at 80°C.

are collected. This equation has the form of a straight line with the y-intercept equal to the actual quantum efficiency and the slope proportional to the lateral collection distance. Both the quantum efficiency and the lateral collection distance decreased after bakeout, as seen in Fig. 3, but the lateral collection distance (which is proportional to the minority carrier lifetime) decreased by a greater amount (more than a factor of two).

To confirm that a lifetime variation is responsible for parameter degradation after bakeout, direct lifetime measurements were performed on the four quarters of the single n-layer wafer, before and after vacuum bakeout for 240 h at 80°C. The measurement results shown in Fig. 4 show a significant lifetime degradation (more than a factor of three) after bakeout for the sample "S" (standard process sequence), a result which is consistent with the above mentioned parameter degradation.

Because dark current and impedance degradation were sufficient only for small area devices where the perimeter-to-area ratio is very high, meaning the diodes are highly sensitive to surface quality, surface defect generation was presumed to be the cause of this degradation.

Analysis of the R_0A_{opt} product as a function of photodiode junction area has been performed to determine if surface or bulk effects are responsible for bakeout degradation.[4,5] As seen in Fig. 5, for devices fabricated using the standard process, diodes which showed bulk defect limited performance before the bakeout became surface limited after bakeout.

Devices Fabricated with Post-Passivation Anneal

It is thought that some kind of defect, possibly Hg vacancies, is being generated at the CdTe/HgCdTe interface during the long-term elevated temperature bakeout. To prevent the incorporation of electrically active Hg vacancies, a post-passivation anneal under high Hg pressure was performed for both the single n-layer and photodiode test structures. Fabricated devices were then subjected to the 240 h vacuum bake at 80°C and measured.

The measurement results on Hg annealed samples are summarized as follows:

- For the photodiode test structures, zero and reverse bias impedance (Fig. 6) and dark current (Fig. 7) did not degrade for all size diodes. In this case, both small and large diodes showed the same kind of performance.
- Quantum efficiency and lateral collection distance (Fig. 8) were the same before and after bakeout.
- For the n-layer samples annealed after CdTe passivation ("B" and "C"), the minority carrier lifetime did not change after bakeout (Fig. 4). However, the part of the wafer annealed before passivation ("D") showed the same lifetime degradation as the standard process part.
- For the photodiode test structures, analysis of the R_0A_{opt} product vs photodiode junction area (Fig. 9) confirmed bulk defect limited photodiode performance both before and after bakeout.

Thus, it was confirmed that annealing at 220°C under Hg vapor, after CdTe passivation deposition, suppressed surface defect generation and significantly improved the bake stability performance.

CONCLUSION

It was found that defects are created at the CdTe/HgCdTe (LPE-grown with n-layer doping of 1×10^{15}) interface during a 240 h bakeout at 80°C under vacuum for wafers with LWIR photodiodes passivated by a technique based upon thermal evaporation of CdTe. These defects (which are believed to be electrically active Hg vacancies) degrade the minority carrier lifetime, as well as photodiode zero bias impedance, dark current and photo response. A Hg anneal treatment after CdTe passivation has been shown to prevent the incorporation of electrically active Hg vacancies and significantly improve photodiode stability for bakeout similar to conditions used for preparation of tactical dewar assemblies.

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